



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cheng, *et al.* Attorney Docket: TSM03-0549  
Filed: Herewith Examiner: TBD  
Serial No.: 10/749,080 Art Unit: TBD  
For: Depletion-Merged FET Design in Bulk Silicon

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & 08B that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

6 April 04  
Date

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Approved for use through 07/31/2006. OMB 0651-0031

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

**Complete if Known**

Application Number	10/749,080
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Filing Date	December 30, 2003
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First Named Inventor	Cheng <i>et al.</i>
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Art Unit	TBD
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Examiner Name	TBD
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Sheet	1	of	2	Attorney Docket Number	TSM03-0549
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## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

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Examiner Signature		Date Considered	
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PTO/SB/08b (08-03)

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**INFORMATION DISCLOSURE  
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Sheet

2

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**Complete if Known**

Application Number 10/749,080

Filing Date December 30, 2003

First Named Inventor Cheng *et al.*

Art Unit TBD

Examiner Name TBD

Attorney Docket Number TSM03-0549

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		ERTL, FRANK <i>et al.</i> , "Vertical transistors with ultra-short channel lengths," <i>Fundamental research in semiconductor electronics - Annual Report 2000</i> , (2000) pp. 90-91.	
		GÖHLER, LUTZ. <i>et al.</i> , "A Compact Model for Depletion MOSFETs in Smart Power Applications Including Source and Drain Resistance," (Date Unknown) 5 pages.	
		MANNERS, DAVID, "Infineon Looks to NROM," <i>Electronics Weekly</i> , (May 28, 2001) <a href="http://www.reed-electronics.com/electronicnews">http://www.reed-electronics.com/electronicnews</a> .	
		SHEPARD, KENNETH, <i>et al.</i> , "Static Noise Analysis for Digital Integrated Circuits in Partially-Depleted Silicon-On-Insulator Technology," <i>Proceedings of the Design Automation Conference</i> , Los Angeles, California, (June 2000) 4 pages.	
		STOCKINGER, MICHAEL, "2.3 Drain-Induced Barrier Lowering," (January 05, 2000) <a href="http://www.iue.tuwien.ac.at/phd/stockinger/node15.html">http://www.iue.tuwien.ac.at/phd/stockinger/node15.html</a> .	

Examiner  
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Date of Deposit: April 6, 2004

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Information Disclosure Statement (1 page)  
Form PTO/SB/08A & 08B with 7 References Cited (2 pages)  
Copy of 5 References Cited  
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Respectfully submitted,

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